Claim 1 (currently amended): A method of fabrication of an integrated circuit, comprising the steps of:

(a) patterning a first layer of resist on a layer of antireflective coating comprising a silicon oxynitride material and which is on a layer of gate material to define gate locations;

(b) reducing the linewidth of said patterned layer of resist of step (a);

(c) using said reduced linewidth patterned resist as an etch mask to form gates from said layer of gate material;

(d) forming a layer of dielectric on said gates;

(e) patterning a second layer of photoresist on a second layer of antireflective coating comprising a second silicon oxynitride material to define interconnects;

(f) using said patterned photoresist without linewidth reduction to form interconnects over said gates.

Claim 2 (original): The method of claim 1, wherein:

(a) said using of step (f) of claim 1 is using the patterned photoresist as an etch mask for an underlying layer of metal.

Claim 3 (original): The method of claim 1, wherein:

(a) said using of step (f) of claim 1 is using the patterned photoresist as an etch mask to etch grooves in underlying dielectric to be filled with metal.

Claim 4 (currently amended): A method of fabrication of an integrated circuit gate, comprising the steps of:

(a) patterning a first layer of resist on an antireflective layer of a first silicon oxynitride material on a layer of dummy gate material to define gate locations;

(b) reducing the linewidth of said patterned layer of resist of step (a);

(c) using said reduced linewidth patterned resist as an etch mask to form dummy gates from said layer of dummy gate material;

(d) forming a layer of dielectric adjacent said dummy gates;

(e) removing said dummy gates;

(f) depositing gate material on said dielectric and

(g) patterning a second layer of photoresist on a second antireflective layer of a second silicon oxynitride material on said gate material to define gates;

(h) using said patterned photoresist without linewidth reduction to form gates.

Claim 5 (new): A method of fabrication of an integrated circuit, comprising the steps of:

(a) patterning a first layer of resist on a first layer of antireflective coating comprising a first silicon oxynitride material and which is on a layer of gate material to define gate locations;

(b) using said patterned resist of step (a) as an etch mask to form gates from said layer of gate material;

(c) forming a layer of dielectric on said gates;

(d) patterning a second layer of resist on a second layer of antireflective coating comprising a second silicon oxynitride material to define interconnects;

(e) using said patterned resist of step (d) to form interconnects over said gates.

Claim 6 (new): The method of claim 5, wherein:

(a) said using of step (e) of claim 5 is using the patterned resist as an etch mask for an underlying layer of metal.

Claim 7 (new): The method of claim 5, wherein:

(a) said using of step (e) of claim 5 is using the patterned resist as an etch mask to etch grooves in underlying dielectric to be filled with metal.